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Design and Analysis of 4-Bit Adder Using Distinctive Approaches in Cadence 45nm Technology

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ABSTRACT: The Adder plays a crucial role in any processor/controller design. As of now there are plenty of 4-bit fulladders proposed and designed. In this paper we have an analytic description of various full adder circuits (GDI, SERF), considering various constraints like power, performance and area. The circuits are designed in Cadence Virtuoso, GPDK 45nm technology. The Full adder circuits with the most 112 transistors to the one with only 40 transistors are successfully designed and simulated for various parameters like power consumption, speed of operation (delay) and area (transistor count). It adds the two four binary values and is the main part for other operations such as subtraction (complement addition), multiplication (successive addition), division (successive subtraction), etc. Overall performance of the digital system will be reflected in the adder circuits. Static Energy Recovering Full adder (SERF) logic design is used to implement the design with XOR and XNOR gates and balancing the delays of output gates. Gate Diffusion Input (GDI) is a technique to reduce the dynamic and static power dissipation in digital systems. Comparing with conventional Full adder our proposed circuits prevail least power.

KEYWORDS: Full adder, GDI, SERF, Cadence Virtuoso

I. INTRODUCTION

In recent times, VLSI applications such as audio and video processing, microprocessors, and digital signal processing have relied heavily on arithmetic operations. In the past, VLSI designs were primarily focused on factors such as area, reliability, and cost rather than power consumption. However, with the growing demand for electronic devices such as mobile phones, laptops, and other portable devices that require high speed and low power consumption, power has become a critical factor in VLSI designs. The high power consumption of portable devices is a major challenge for the semiconductor industry as it leads to a shorter battery life and can cause silicon parts of the devices to fail. Additionally, controlling heat levels in these devices requires high packaging costs and cooling arrangements that consume less power. Hence, the need for low-power devices has become critical in the semiconductor industry. To achieve low power consumption, various techniques such as reducing the supply voltage, dynamic voltage scaling, clock gating, power gating, and multi-Vt designs are being used in VLSI designs. These techniques help reduce power consumption while maintaining or improving performance. Another important consideration in low-power VLSI designs is reducing the critical path delay of the devices. This can be achieved through optimizing device architecture and using appropriate circuit design techniques. By reducing the critical path delay, devices can achieve high-speed processing while consuming minimal power, making them suitable for use in portable and battery-operated electronic devices. Power dissipation in electronic devices is typically categorized into two types: static power dissipation and dynamic power dissipation.

Static power dissipation is caused by sub threshold leakage and short-circuit transistor current leakage, which can be reduced by resizing CMOS transistors.

Dynamic power dissipation, on the other hand, is mainly due to the switching activity of transistors during charging and discharging.

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Power dissipation can be minimized at different levels of design, such as at the architectural, algorithmic, gate-level, or circuit-level. In this paper, we aim to minimize power dissipation at the transistor level by designing and modifying existing adder circuits with different topologies. 4-Bit Full adder circuits with varying numbers of transistors have been used in the design of these circuits analysis of power. we will determine the best design for specific applications. By modifying existing designs and exploring new topologies, we aim to reduce power dissipation and improve the overall efficiency of electronic devices.This paper is structured into some sections.

In the next section, we will provide an overview of the existing and proposed designs of various full adders. Section 3 will explain the process of capturing these designs and how we modified them to achieve better performance in terms of power dissipation .In Section 4, we will present the results of our simulations by implementing the modified designs using the Cadence tool. We will provide a detailed analysis of the performance of each designs. Finally, in Section 5, we will conclude our project by summarizing the key findings of our research and highlighting the limitations of our approach. We will also discuss future work.

II. EXISTING AND PROPOSED ADDER DESIGNS

Here different 4-Bit full adder are considered for power analysis .Namely 40T GDI 4bit full adder design, 40T SERF 4bit full adder design.

A. Basic 4-Bit full adder design

The basic 4-Bit full adder design has 9 input bits with the addition of this bits gives output as S0,S1,S2,S3 and carry. This is basic model of 4 bit adder design to design different topologies.

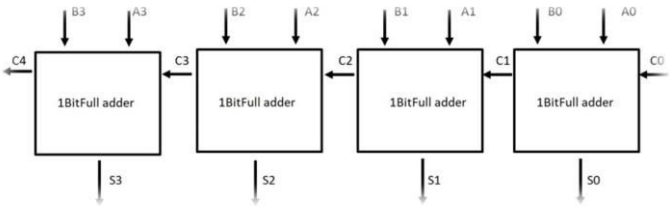

Fig.1 Basic 4-bit full adder

B. 10TGDI 1Bit Full adder design

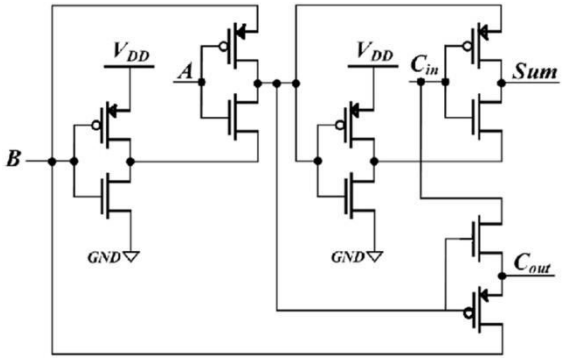

Fig.2 Basic 10T GDI full adder

The Gate Diffusion Input Full adder design you described is a valid design technique for implementing a full adder using CMOS logic. Firstly, you mentioned that the full adder has 3 inputs and 2 outputs, which is incorrect. A full adder has 3 inputs (A, B, and carry-in) and 2 outputs (sum and carry-out). Secondly, it is not clear what you mean by "4 terminals". A typical CMOS transistor has 3 terminals - gate, source, and drain. It would be helpful if you could clarify which specific terminals you are referring to. Thirdly, the sentence "N or P are connected using bulk amount of both

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NMOS and PMOS transistors" is not clear. It is unclear what you mean by "bulk amount" and how the N and P transistors are connected.

C. 10T SERF 1Bit Full Adder Design

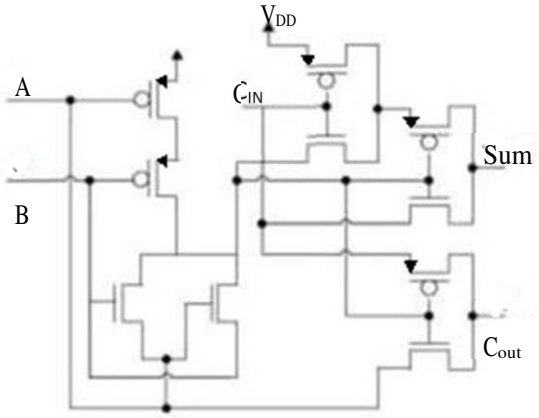

Fig.3 Basic 10T SERF full adder

The Static Energy Recovering Full Adder logic design is a useful technique for implementing a Full Adder with XOR and XNOR gates while balancing the delays of the output gates. The design reduces power consumption by not having a direct path to ground and reusing the charge stored in a load capacitance. However, this design has some disadvantages that need to be addressed. One of the main issues with this design is that the output nodes have full swings, which can lead to power supply problems at the internal nodes.. In summary, while the Static Energy Recovering Full Adder logic design is an efficient way to store energy and reduce power consumption. By using techniques such as level-shifting, biasing, transistor sizing, or dynamic voltage scaling, the design can be made more robust and reliable in the face of variations in temperature and process.

D. 4-Bit GDI Full adder design

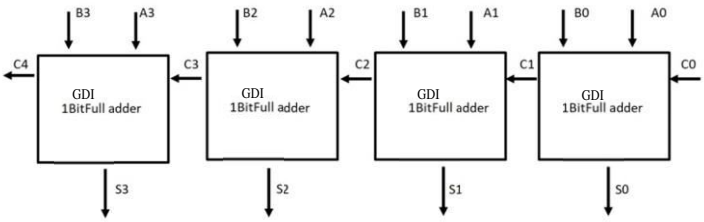

Fig.4 40T GDI full adder

A 4-bit full adder can be implemented using the Gate Diffusion Input (GDI) technique. The GDI technique is a low-power design methodology that utilizes a combination of logic gates and transistors to reduce power consumption. To implement a 4-bit full adder using GDI, we would need 4 full adders, each of which would have 3 inputs (A, B, and carry-in) and 2 outputs (sum and carry-out). The carry-out from each full adder would be connected to the carry-in of the next full adder in the sequence. Each full adder can be implemented using a combination of GDI XOR, XNOR, and NAND gates, along with PMOS and NMOS transistors. The GDI gates are used to perform the logical operations, while the PMOS and NMOS transistors are used to control the flow of current through the circuit. The GDI technique allows for the implementation of low-power designs, as it reduces the number of transistors required to perform a logical operation. Additionally, the GDI technique can help balance the delay of output gates, which can lead to improved performance and reduced power consumption. In summary, a 4-bit full adder can be implemented using the GDI technique, which utilizes a combination of logic gates and transistors to reduce power consumption and improve performance.

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E. 4-Bit SERF Full adder design

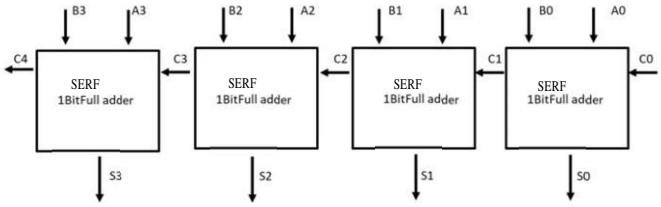

Fig.5 40T SERF full adder

A 4-bit SERF (Static Energy Recovering Full adder) Full Adder is a type of full adder that uses a feedback mechanism to improve its performance. The SERF Full Adder is designed to have faster switching speed and higher power efficiency compared to a conventional full adder. The 4-bit SERF Full Adder can be implemented by cascading four SERF Full Adders together. Each SERF Full Adder consists of two stages – a pre-charge stage and a computation stage. In the pre-charge stage, the input signals are applied to the gates of PMOS and NMOS transistors to pre-charge the internal nodes of the full adder. This stage ensures that the internal nodes are charged to their correct levels before the computation stage begins. In the computation stage, the pre-charged internal nodes are discharged through a feedback mechanism that improves the switching speed and power efficiency of the full adder. The feedback mechanism uses a SERF (Static Energy Recovering Full adder)latch to store and amplify the voltage difference between the internal nodes of the full adder. The output of the SERF latch is fed back to the input of the full adder, which helps to reduce the voltage swing and improve the switching speed. In summary, a 4-bit SERF Full Adder is a type of full adder that uses a feedback mechanism to improve its performance. The SERF Full Adder is designed to have faster switching speed and higher power.

III. SCHEMATIC DESIGN AND SIMULATION

A. 10T GDI Full Adder Design Using Cadence

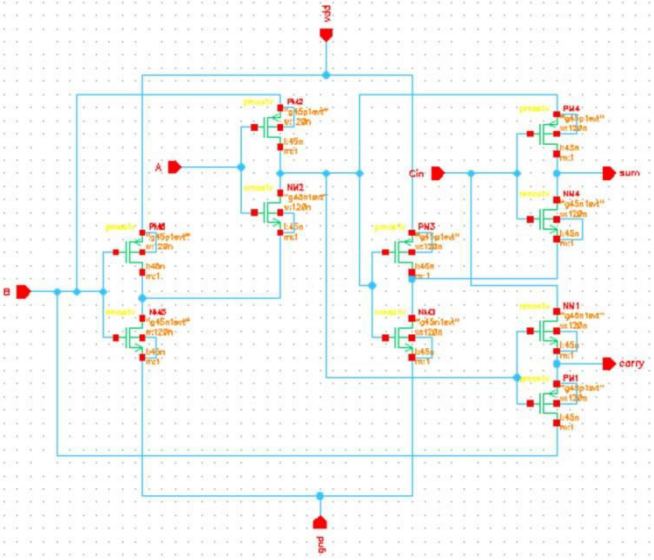

Fig.6 schematic of 10T GDI

The schematic of 10T GDI adder using cadence virtuoso 45nm technology is shown above the diagram. The length of the transistors is 45nm but width varies. The output of the trans analysis is given blow.

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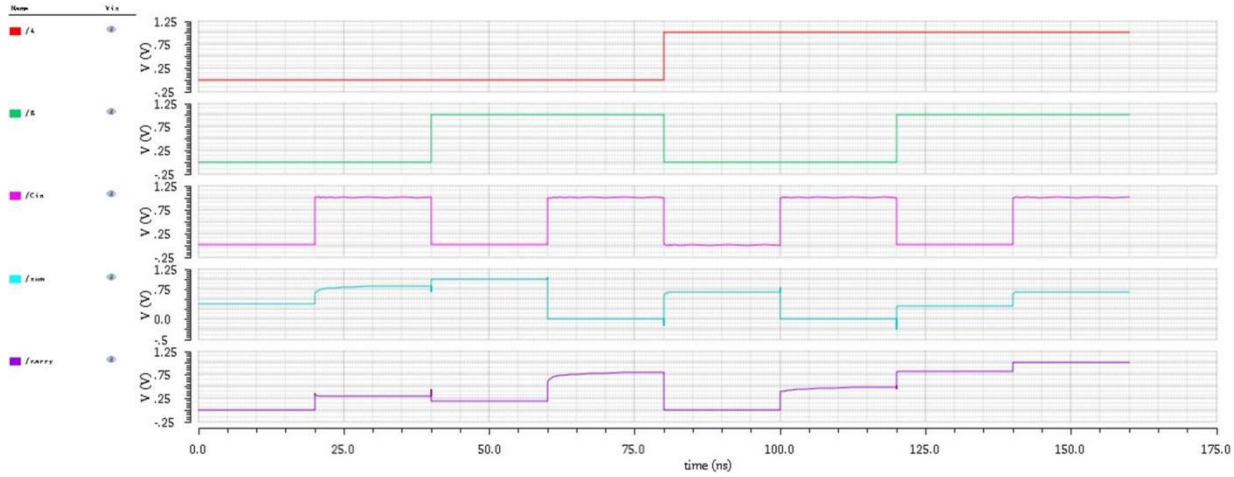

Fig.7 trans analysis of 10T GDI

B. 10T SERF Full Adder Design Using Cadence

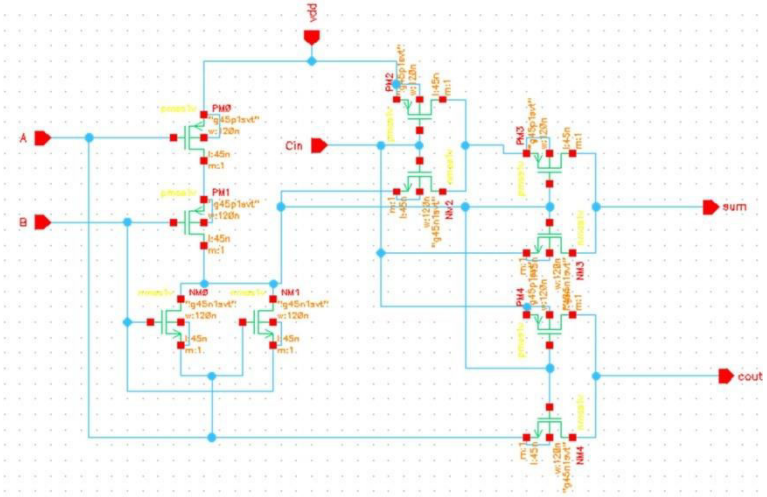

Fig.8 schematic of 10T SERF

The schematic of 10T SERF adder using cadence virtuoso 45nm technology is shown above the diagram. The length of the transistors is 45nm but width varies. The output of the trans analysis is given.

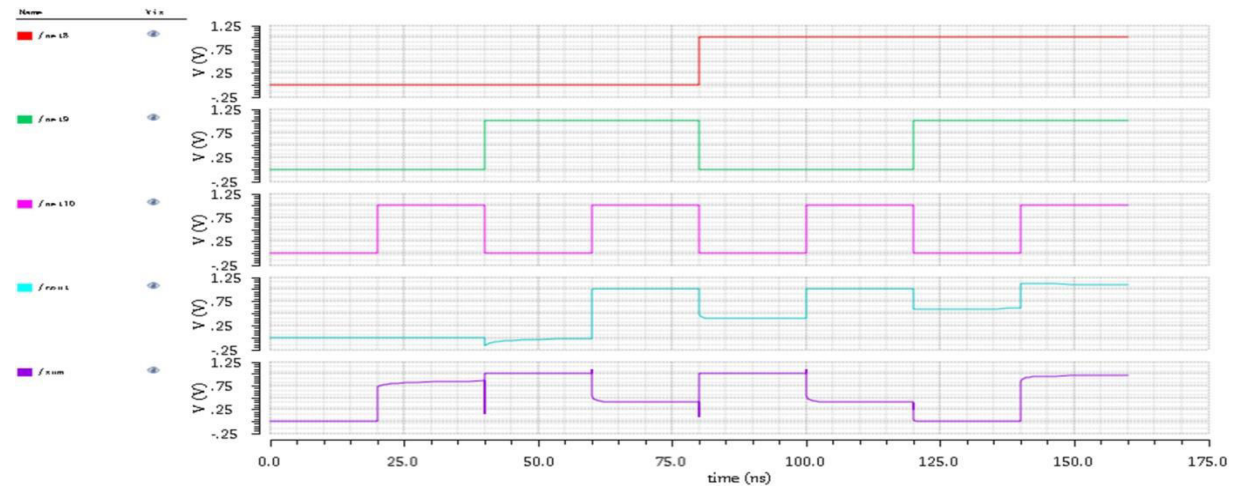

Fig.9 trans analysis of 10T SERF

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C. 40T GDI 4-Bit Full Adder Design Using Cadence Virtuoso

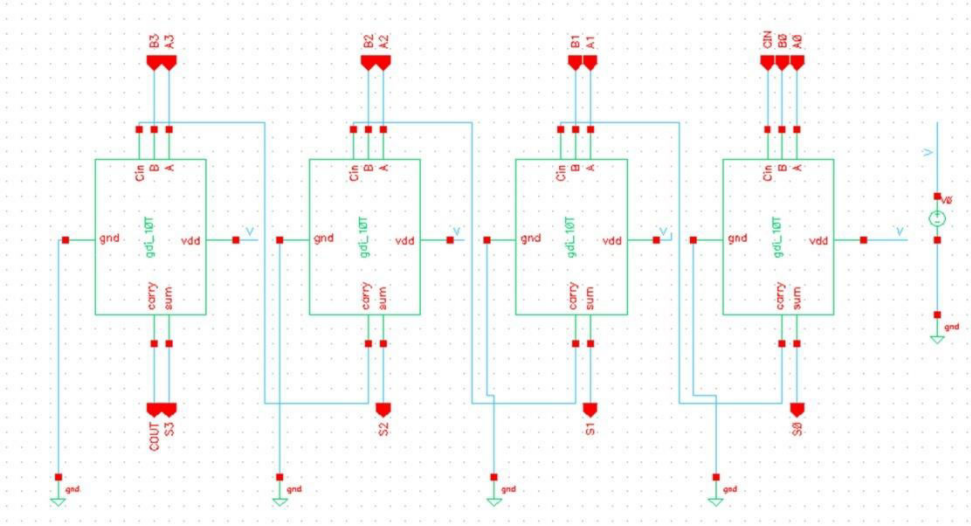

Fig.10 schematic of 40T GDI

The 40T GDI 4-bit full adder is using cadence tool 45nm technology the schematic is shown above the length of the transistor is 45nm. The test bench and output of the circuit is given blow.

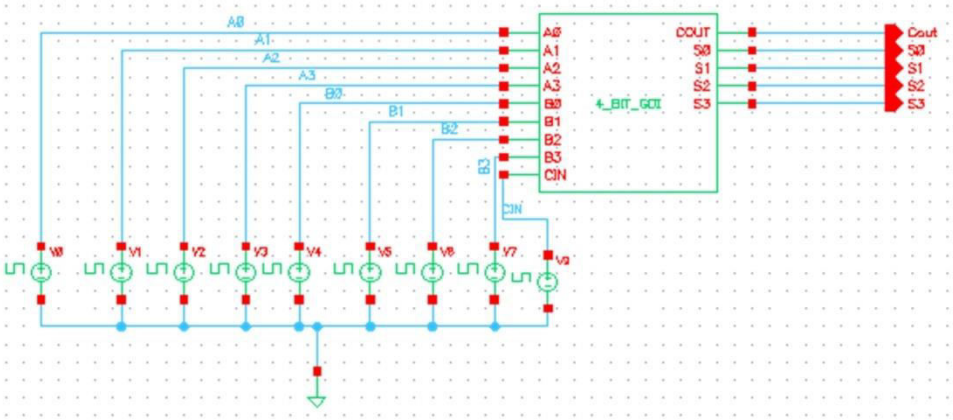

Fig.11 Test bench of 40T GDI

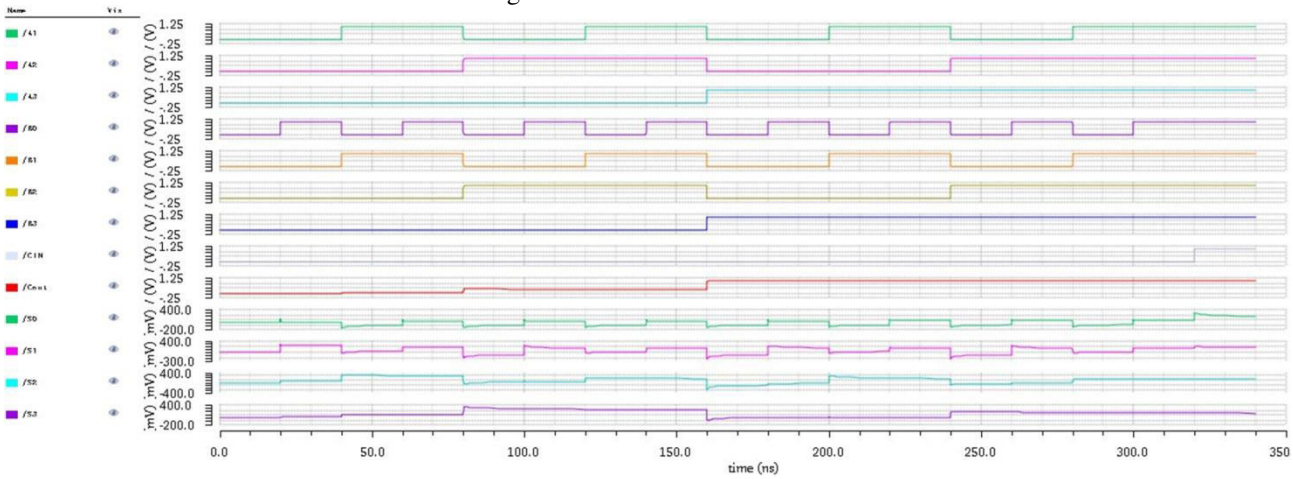

Fig.12 trans analysis of 40T GDI

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D. 40T SERF 4-Bit Full Adder Design Using Cadence

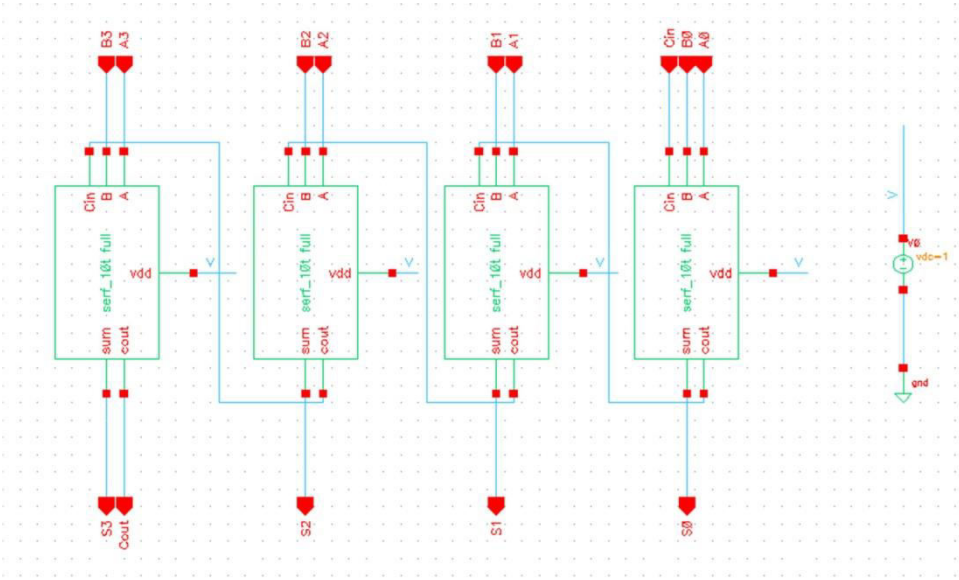

Fig.13 schematic of 40T SERF

The 40T SERF 4-bit full adder is using cadence tool 45nm technology the schematic is shown above the length of the transistor is 45nm. The test bench and output of the circuit is given blow.

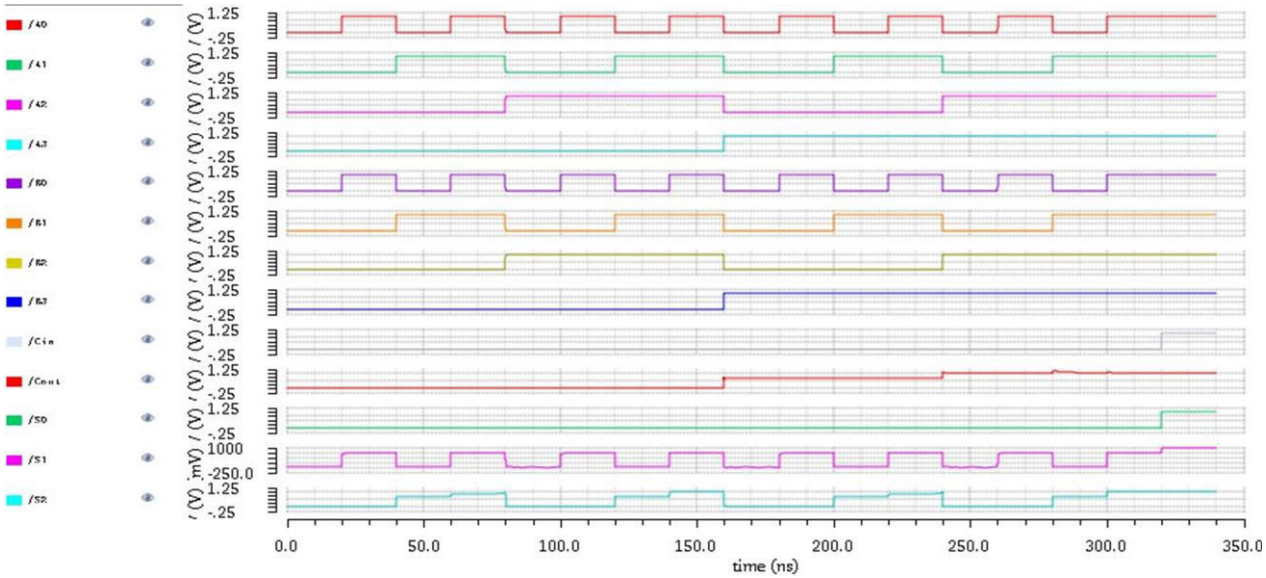

Fig.15trans analysisof40TSERF

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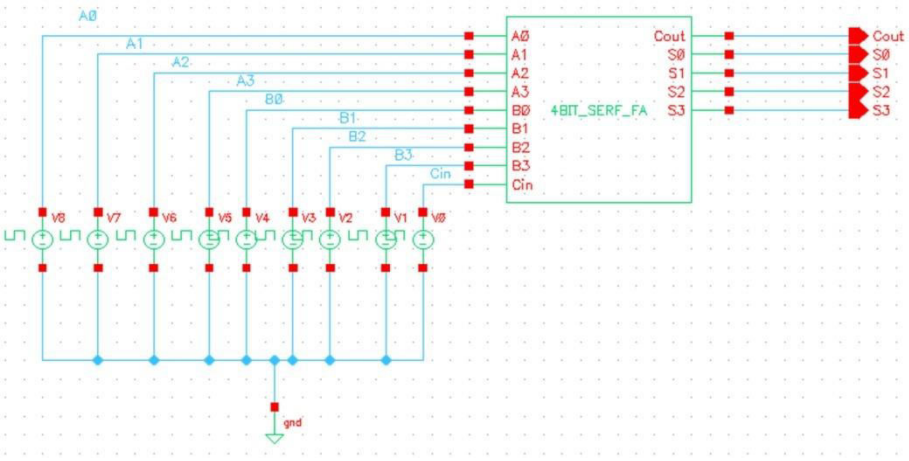

Fig.14 Test bench of 40T SERF

IV. RESULTS

Comparative power analysis of 40T GDI 4-Bit full adder and 40T SERF 4-Bit full adder designs, power shown in the table.

Adders	Technology	Avg. power
GDI 4-Bit full adder	45nm	$9.499E^{-6}$
SERF 4-Bit full adder	45nm	$697.7E^{-9}$

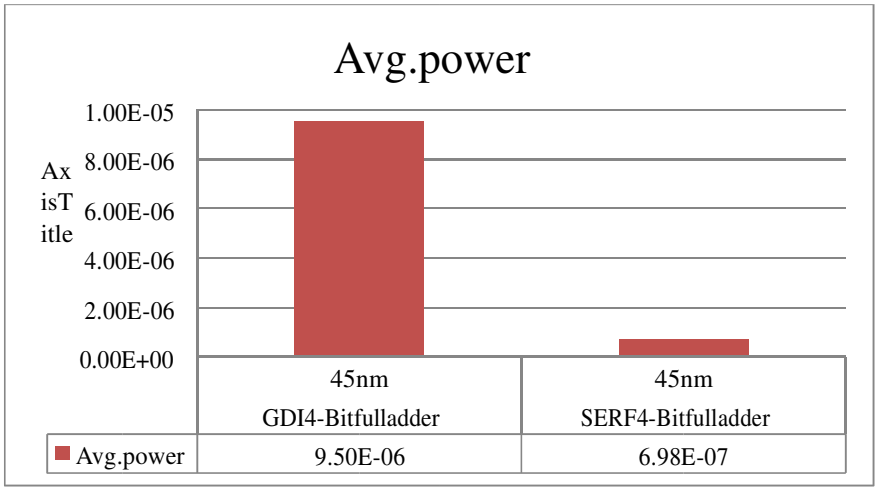

Fig.16Comparison of 4 bitfulladders Power

From the above analysis 40T SERF(Static Energy Recovering Full adder) consumes less power.

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V. CONCLUSION AND FUTURE SCOPE

This project finally concludes that 10T GDI and SERF technique is best in all measurements with low power. In future, we are going to improve the design and take it to post layout. We can compare those adder in various nanometer technologies like 90nm, 180nm. And compare the area, delay of the 4-Blt full adders.

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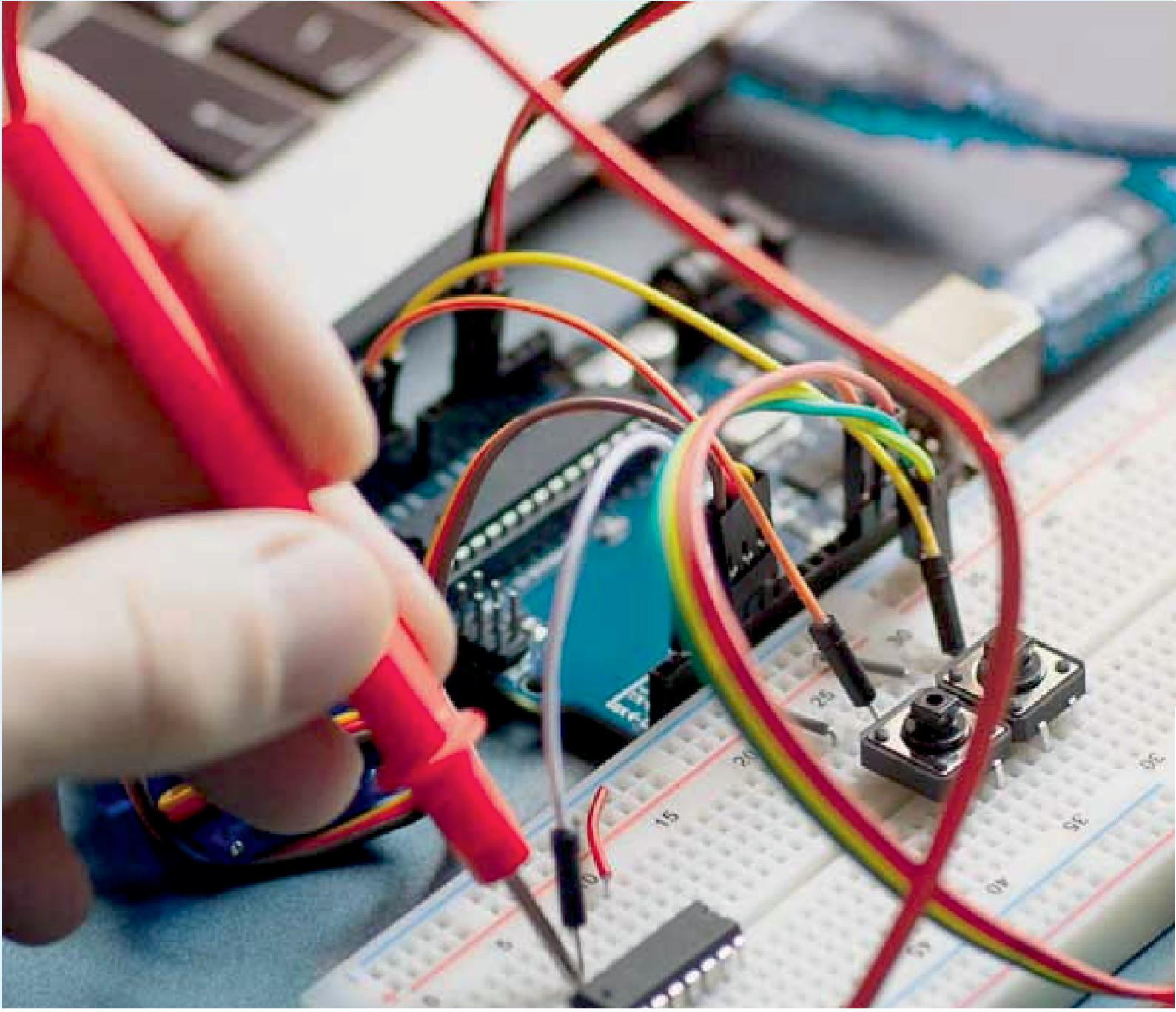

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